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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,849	12/21/2001	Atsushi Yagishita	04329.1949-01000	4501

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EXAMINER	
ROSE, KIESHA L	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,849	YAGISHITA ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- Th MAILING DATE of this communication app ars on th cov r sheet with the corr spond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 30-38 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 June 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to the amendment filed 30 June 2003.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the insulating film formed on the bottom and side surface of the gate wiring layer, the gate electrode and gate wiring layer having a bottom surface lower than the source and drain diffusion layer, gate electrode, gate wiring layer, source electrode and drain electrode having an upper surface level equal to each other, the gate wiring layer connected to the device isolation insulating film and the gate electrode and a connection wire connected to either the gate, source or drain electrode or the gate wiring layer and having an upper surface lower than the device isolation insulating film must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Rejections - 35 USC § 112

Claims 30-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 30-36 disclose an insulating layer formed on the bottom surface and side surface of the gate wiring layer, it is unclear how that is suppose to be formed since the drawings do not disclose this limitation, the gate

electrode, gate wiring layer, source and drain electrodes having an upper surface lower than or equal to the upper surface of the device isolation insulating film, it is unclear how the gate wiring layer is going to have an upper surface equal to or lower than the device isolation film if it is connected to the device isolation film, it is also unclear how the gate wiring layer and gate electrode have a bottom surface lower than the source and drain diffusion layers since the drawings do not disclose this limitation and how is the wiring layer having a bottom surface lower if it is formed on the device isolation and the gate electrode, in addition it is also unclear how the gate electrode, gate wiring and source and drain electrodes could have upper levels equal to each other if the gate wiring layer is formed on the gate electrode it would always be higher than the gate electrode and it is unclear how the connection wiring is formed on the either the gate electrode, gate wiring layer or source and drain electrodes and have an upper surface equal to or lower than the device isolation layer.

Claims 37-38 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 37-38 disclose a pair of thin films formed on the sides of the gate wiring layer, it is unclear what the thin films are or what they are made of and in addition the claimed limitation as shown in the drawings is etched away so therefore there is not thin film in the final product.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 30-36, as far as understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (U.S. Patent 5,482,888).

Hsu discloses a transistor (Fig. 2h) that contains a substrate (40), a device isolation insulating film (54) formed on one major surface of the substrate, a gate electrode (56) formed on one major surface of substrate with an insulating film (55/58) formed on the bottom and side surface of the gate electrode, a gate wiring layer (55) formed on device isolation insulating film and connected to the gate, a source diffusion layer (64), a drain diffusion layer (66), a source electrode (60) and a drain electrode (62).

Claims 37 and 38, as far as understood, is rejected under 35 U.S.C. 102(e) as being anticipated by Applicant's Prior Art.

Applicant's Prior Art (Fig. 2b) discloses a semiconductor device that contains a substrate (1), a gate wiring layer (3) formed on one major surface of the substrate, an insulating film (2/10) formed between the substrate and gate wiring layer and on the

side surface of the gate wiring layer, a gate sidewall (4) formed on the side surface of the gate wiring layer made of a insulator.

Response to Arguments

Applicant's arguments filed 30 June 2003 have been fully considered but they are not persuasive. Applicant's arguments in regards to the 112 rejections do not clearly overcome the previous rejection. The limitations that are described in the 112 rejections clearly state what the discrepancies are and the arguments state something different as the reasons to overcome the rejection, for example the rejection states that the gate wiring layer and gate electrode have a bottom surface lower than the source and drain diffusion layers it is unclear how this is done and the drawings do not disclose these limitations and the response back was that the claims do not recite "the gate wiring layer formed on the device isolation insulating film and the gate electrode" but they recite " a gate wiring layer formed in said device isolation insulating film" The rejection did not state anything about a device isolation insulating film and therefore does not answer the questions raised by the 112 rejections. Therefore the rejection stands. In regards to the drawings the drawings still do not show the gate electrode and gate wiring layer having a bottom surface lower than the source and drain diffusion layer, gate electrode, gate wiring layer, source electrode and drain electrode having an upper surface level equal to each other.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 703-605-4212. The examiner can normally be reached on M-F 8:30-6:00 off 1st Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

KLR
September 23, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800